A Protective and Measure Device for Multiple Cold Cathode Fluorescent Lamps

Field of the Invention

The preferred embodiment is employed as the backlighted display of large- or super-size LCD monitors, which requires parallel connection of multiple cold cathode fluorescent lamps (CCFLs) as light source. The high-frequency power source is typically supplied by an electronic ballast or power exchanger to ensure multiple cold cathode fluorescent lamps of single task working frequency, circuit stability, brightness efficiency, high quality and low distortion. The preferred embodiment provides measuring to such ends and serves as a protective device.

Background of the Invention

Typically application of CCFL as the backlighted display of LCD monitors, calls for an inverter and one or two CCFLs; when employed on large LCD monitors or large LCD TV screens, five to ten inverters may be required that will ensue the following drawbacks:

1. In case one of the tens of CCFLs is defective, the fault cannot be effectively detected, resulting in affecting LCD monitor quality;
2. As variations in high frequency exist among the inverters producing multiple frequency interferences to the LCD monitor, it increases the cost to introduce electromagnetic interference purging;
3. As multiple inverters' high-frequency voltage outputs will invariably vary, the brightness of CCFLs will be inconsistent, thus affecting the LCD monitor quality;
4. Cost of employing multiple inverters is higher than single electronic ballast or a single inverter.

Thus, addressing foregoing deficiencies of typical application of CCFL as the backlighted display of LCD monitors, an innovative solution is proposed: A type of device functioning to measure and protect the circuits of CCFLs is designed so that when any one of tens of CCFLs faults, said device can effectively detect the defect to maintain the LCD monitor quality, while concurrently solving the typical multi-inverter practice's drawbacks of frequency interference, structural

complexity and unnecessary high cost. These problems have long awaited for solutions by users and the author alike. After years of electronics related studies together with field research and development experience, aspiration arises to come up with an efficient solution, thus after repeated designing, investigating, model making and improving, a superior type of electronic device for measuring and protecting the circuits of CCFL has been designed specifically to address said problems.

Summary of the Invention

To effectively provide for the backlighted display required of large- or super-size LCD monitors:

The first objective of the claim is to provide a device for measuring and protecting CCFLs to solve the deficiencies of typical multiple-inverter application.

The second objective of the claim is to employ electronic ballast as a single high-frequency power source to solve typical multiple-inverter application's deficiencies of frequency interference and high cost.

The third objective of the claim is to provide for the backlighted display required of large- or super-size LCD monitors, LCD TV screens, and LCD advertising mediums.

The fourth objective of the claim is to present superior hardware circuits to prove capability of attaining the claimed purposes and efficacy, and as the basis for relevant applications.

To ascertain the deficiencies of typical multiple-inverter employment on large LCD monitors, the claim is characterised by the following features:

1. The measure element parallel connected to each CCFL of a plurality of CCFLs (hereinafter called "CCFL Cluster"), pending on the CCFL's characteristics and requirements may employ a single high-voltage (HV) precision resistor, or a plurality of diodes, or Zener diode.
2. The photocoupler pending upon requirement may be a general photocoupler or photothyristor coupler; the primary is LED, the secondary transistor or thyristor. The power source of the primary is supplied by the voltage of the two ends of the measure element parallel

connected to a single CCFL and through limit current resistor, characterised by each CCFL's secondary being serially coupled.

3. To boost the photocoupler's primary sensitivity, pending upon requirement may employ full-wave rectifier circuit or digital comparator integrated circuit (DCIC), subjecting the AC positive terminal and the AC negative terminal passing through limit current resistor to connect to photocoupler's primary.

4. Because of the photocoupler, CCFL is isolated from the up, down limit comparators, or differential amplifier integrated circuit (DAIC), or DCIC, so prevented from mutual interfering; the requirement of isolation voltage may be met with choice of photocoupler.

5. The up, down limit comparators, or ACIC, or DCIC on the protect circuit ca function to initiate "on", "off" of CCFL Cluster, and over current triggered by HF power source's voltage surge, and comparison of settings of under current triggered by under HF voltage, to attain the objective of protecting and enhancing light source quality.

6. The time delay circuit is characterised by when the electronic ballast is functioning stably and that the CCFL Cluster is fully and stably on, the time required for the up, down limit comparators, or ACIC, or DCIC to output to the HF power circuit's initiate thyristor to determine the on/off state of HF power circuit; the time delay circuit's time delay initiate time is determined by the CCFL Cluster's number, characteristic and quality.

7. Power input of the power supply may be from HF power circuit's AC power or HF power circuit's HF oscillator circuit; the output AC power source is supplied to the protect circuit and the time delay circuit.

8. HF power circuit employs full- or half-bridge type electronic ballast equipped with single HF power source, sufficient HF output function, single output voltage, brightness control, working frequency adjustment, start control and protection against irregularities.

Brief Description of the Drawings

Fig. 1 is the block chart of the claimed device;

Fig. 2 is the claimed device's superior schematic implemented;

Fig. 3 is the first exemplary schematic of claimed CCFL measure and protective device;

Fig. 4 is the second exemplary schematic of claimed CCFL measure and protective device;

Fig. 5 is the third exemplary schematic of claimed CCFL measure and protective device;

Fig. 6 is the fourth exemplary schematic of claimed CCFL measure and protective device;

Fig. 7 is the fifth exemplary schematic of claimed CCFL measure and protective device;

Fig. 8 is the sixth exemplary schematic of claimed CCFL measure and protective device;

Fig. 9 is the seventh exemplary schematic of claimed CCFL measure and protective device;

Fig. 10 is the eighth exemplary schematic of claimed CCFL measure and protective device;

Fig. 11 is the ninth exemplary schematic of claimed CCFL measure and protective device;

Fig. 12 is an alternative connection to Fig. 8 schematic equipped with balance resistor VR;

Fig. 13 an alternative connection to Fig. 9 schematic equipped with balance resistor VR;

Fig. 14 is the tenth exemplary schematic of claimed CCFL measure and protective device;

Fig. 15 is the eleventh exemplary schematic of claimed CCFL measure and protective device;

Fig. 16 is the twelfth exemplary schematic of claimed CCFL measure and protective device.

Detailed Description of the Preferred Embodiment

As shown in Fig. 1, the block chart of the claimed device consists of: CCFL Cluster protect circuit 100, HF power circuit 200, time delay circuit 300, and DC

power circuit 400.

Fig. 2 is the claimed device's superior schematic implemented; HF power circuit 200 is a type of electronic ballast driven by AC power, primarily structured on regular half- or full-bridge type oscillator circuit; the HF oscillator voltage passes through the primary coil of HF transformer, while the secondary coil detects a high voltage (HV) at AB terminal, connected with L1, L2, L3....Ln cold cathode fluorescent lamps (collectively called "CCFL Cluster"); whereof Lo represents another CCFL Cluster and protect circuit, thus the circuit consists of two clusters. Naturally to meet with the requirement of backlighting super-size LCD screens, multiple clusters may be conjoined. Additionally a HF oscillator voltage passes the primary coil of HF transformer, while the secondary coil detects the input terminal of a low voltage (LV) supply to DC power circuit 400, and the output DC voltage supplies to CCFL Clusters and protect circuit 100 up, down limit comparators OP1 and OP2 (or DAIC or DCIC), an time delay circuit 300, or power supply by other independent system. HF oscillator circuit 210 is controlled by thyristor silicon control rectifier (SCR) so that when the output of up, down limit comparators OP1 and OP2 is positive, thyristor SCR 220 will be triggered, HF oscillator circuit 210 will stop oscillation; at this time CCFL Clusters have no HF power source, and the backlighting function ceases.

Fig. 3 is the first exemplary schematic of claimed CCFL measure and protective device: from the schematic it is evident that the AB terminal is connected with L1, L2, L3....Ln cold cathode fluorescent lamps; whereby L1, L2, L3 and Ln are of the same circuit; L1 consists of HF HV Capacitor C, cold cathode fluorescent lamp CL, measure resistor R1, limit current resistor R2 and primary of photocoupler. HF HV Capacitor C functions to stabilise HF CCFL flashing; measure resistor R1 adopts HV resistor; the cold cathode fluorescent lamp CL current passes the measure resistor R1 to derive a voltage attenuation; the voltage attenuation's voltage passes through the limit current resistor R2 to the primary of photocoupler Ph1, namely the photocoupler LED terminal, characterised by serial connection of HV Capacitor C and cold cathode fluorescent lamp CL and measure resistor R1; the two terminals are coupled with HF HV terminal, namely AB terminal, and the two ends of measure resistor R1 are parallel connected to the two ends of the LED terminal of photocoupler Ph1after serial connection.

When photocoupler Ph1, Ph2, Ph3...Phn LED receives power supply, the

secondary, namely collect-emitter's two ends will be in 'Turn-on' state; the two ends of photocoupler Ph1, Ph2, Ph3...Phn collect-emitter form serial connection, thus DC power source terminal B+ passes through limit current resistor R30, then passes through collect-emitter serial circuit of photocoupler Ph1, Ph2, Ph3...Phn to reach the up comparator OP1 noninverter terminal and the down comparator OP2 inverter terminal. In this case when comparator OP1 noninverter terminal's voltage is higher than the inverter terminal's set voltage, it indicates that the CCFL Clusters are subjected to overly HF voltage that mitigates the resistance at the collect-emitter of photocoupler Ph1, Ph2, Ph3...Phn, namely causing the measure resistor R1 to have excessive HF current triggered by HF voltage to drive up voltage at the two ends of measure resistor R1, resulting in resistance reduction between collect-emitters, which leads to the up comparator OP1 noninverter's voltage being higher than the inverter. The output end sends out a positive voltage passing through the diode D20, and the limit current resistor R22 to the thyristor SCR220 of the electronic ballast 200 to conduct SCR220: the HF oscillator circuit 210 stops functioning, AB two terminals drained of HF and HV to protect the CCFL Clusters. In the case HF and HV are insufficient at the AB terminal, or one of the CCFL Clusters is "on" or spark occurrence at the two ends of the CCFL Clusters due to poor contact, it will lead to driving up the photocoupler's collect-emitter resistance, and the sparks produced will cause unstable collect-emitter "on" and "off". The positive terminal voltage of the down comparator OP2 is greater than the negative terminal, causing the output terminal to send out a voltage, passing the diode D10, then passing the limit current resistor R12 to reach the thyristor SCR220 of the electronic ballast 200. Thus purging the AB two terminals of HF and HV to protect the CCFL Clusters' function and quality. In this preferred embodiment, the up, down limit comparators may be replaced with DCIC or ACIC.

As shown in Fig. 4 the second exemplary schematic of the preferred embodiment, the measure resistor R1 in the schematic of Fig. 3 is changed to first diode cluster D11 and second diode cluster D22; the remainder of the schematic and functioning principle stays. The second diode cluster D22 consists of multiple diodes, characterised by diodes' positive voltage of about 0.7 volt, i.e., serial connection of five diodes arrives at 0.7 volt x 5 = 3.5 volts, using this voltage to

supply the limit current resistor R2 and the LED terminal of the photocoupler Ph1, meanwhile the first diode cluster D11 is intended to balance the voltage drop of HF voltage during the positive and negative half cycles. The purpose of the circuit is to accommodate the heavy load of the CCFL CL; of which the first and second diode clusters are disposed at the reverse direction. In this preferred embodiment, the up and down limit comparators may be replaced by DAIC or DCIC.

As shown in Fig. 5 the third exemplary schematic of the preferred embodiment, the measure resistor R1 of Fig. 3 is changed to Zener diode Dz; the remainder of the schematic and functioning principle stays. The Zener voltage at the two ends of Zener diode Dz is for supplying the limit current resistor R2 and the LED terminal of the photocoupler Ph1, intended to accommodate small CCFL CL, characterised by simplicity in structure and low in cost. In this preferred embodiment, the up and down limit comparators may be replaced by DAIC or DCIC.

As shown in Fig. 6 the fourth exemplary schematic of the preferred embodiment, to enhance the sensibility of the photocouplers Ph1, Ph2, Ph3...Phn, the two ends of the measure resistor R1 in Fig. 3 schematic are parallel connected to form the AC terminal of a bridge rectifier BR. The DC positive terminal is coupled with the limit current resistor R2 and the LED terminal of the photocoupler Ph1, then connected the DC negative terminal. The power supplying the LED terminal still comes from the two ends of the measure resistor R1, intended to supply full wave voltage at the LED terminal of the photocouplers Ph1, Ph2, Ph3...Phn to boost the sensibility, characterised by serving as suitable backlighting for small CCFL CL or few numbers of CCFLs. In this preferred embodiment, the up and down limit comparators may be replaced by DAIC or DCIC.

As shown in Fig. 7 the fifth exemplary schematic of the preferred embodiment, the measure resistor R1 from Fig. 6 schematic is changed to the first and second diode clusters D11 and D22, same as Fig. 4, the functioning principle is the same as Fig. 4 and Fig. 6, intended for supplying large CCFL and photothyristor, characterised by suitability to photothyristor of lower sensibility. For backlighting super-size LCD screens, photocoupler may be adopted. In this preferred embodiment, the up and down limit comparators may be replaced by DAIC or DCIC.

As shown in Fig. 8 the sixth exemplary schematic of the preferred embodiment, the measure resistor R1 of Fig. 6 schematic is changed to the first and second Zener diode Dz1 and Dz2, the functioning principle is the same as Fig. 6. The voltage for the LED terminal of the photocouplers Ph1, Ph2, Ph3...Phn comes from the Zener voltage of the first and second Zener diode Dz1 and Dz2, intended for backlighting small CCFL cluster, characterised by simplicity in structure, low in cost, and boosted photocoupler sensibility. In this preferred embodiment, the up and down limit comparators may be replaced by DAIC or DCIC.

As shown in Fig. 9 the seventh exemplary schematic of the preferred embodiment, two CCFL clusters share a set of up and down comparators OP1 AND OP2. Among each cluster, one end of every CCFL is coupled together to jointly use a measure resistor R1. The limit current resistor R2, after serially connected to the LED terminal of photocoupler Ph is joined at the two ends of the measure resistor R1. The collect-emitter end of the photocoupler Ph is connected with diodes D30 and D40, while the N-type terminal of D30 and D40 and grounding resistor R3 are coupled to the noninverter and inverter of the up and down comparators OP1 and OP2, the functioning principle is the same as Fig. 3 schematic. In place of the measure resistor R2, two diode clusters D11 and D22, or Zener diode Dz or Zener diodes Dz1 and Dz2 may be used as replacement pending upon requirement. It is characterised by the purpose of reducing the number of photocouplers and up, down comparators. In this preferred embodiment, the up and down limit comparators may be replaced by DAIC or DCIC.

As shown in Fig. 10 the eighth exemplary schematic of the preferred embodiment, two CCFL clusters share the DAIC of a differential amplifier. Among each CCFL cluster, one end of every CCFL is coupled together to jointly use a measure resistor R1. The limit current resistor R2, after serially connected to the LED terminal of photocoupler Ph is joined at the two ends of the measure resistor R1. The mid point of veritable resistor VR and one end of the measure resistor R1 are jointly connected to B terminal. The emitter terminal of the photocoupler Ph is grounded, while the collect-emitter terminal is coupled with the V1 terminal of DAIC and one end of the negative resistor R31, and the other end of negative resistor R31 is connected to B+ power source. The V2 terminal

of the DAIC is connected another CCFL cluster, so that when V1=V2, the output voltage V0 is positive, and concomitantly when the DAIC is V1=V2, the output voltage V0 is zero, pending upon the application without restriction. In this schematic, when the DAIC is V1=V2, the output voltage V0 is positive. During the initial use of the two CCFL clusters, the two CCFL clusters may be adjusted by balance resistor VR, for V1 and V2 to derive equivalent voltage. After using for a while when V1 and V2 become unequal, the output voltage of the V0 is zero, indicating one or multiple lamps of the CCFL cluster deteriorated, closed circuited or shorted, to trigger the protect circuit in achieving the purpose of protection. The V0 output terminal of the DAIC is connected to fork resistors R49 and R50 to reach the base terminal of the transistor T1, while the collector terminal is coupled with a negative resistor R51 as the output terminal, which is then connected to G terminal. The voltage output at the terminal G is opposite to the output voltage of the V0; when V0 is positive and the G terminal is zero (about 0.4v) and V0 is zero, the output of the G terminal is positive. The other end of the negative resistor R51 is connected to B+ power source. The preferred embodiment is characterised by when two CCFL clusters are uneven in number, or the lamp properties are not uniform, it requires only initial tuning of the balance resistor VR for the two lamp clusters to reach voltage equilibrium before application to achieve the purpose of protection. In this preferred embodiment, the DAIC may be replaced with up and down limit comparators.

As shown in Fig. 11 the ninth exemplary schematic of the preferred embodiment, DCIC is used to replace the DAIC of Fig. 10 schematic. The conditions of input terminals V1 and V2 are exactly the same, while the output end comprises three sets: V1>V2, V1=V2, and V1<V2. When V1=V2, its output terminal is positive, passing through a limit current resistor R52 before connecting to the P-type terminal of LED, while the N-type terminal of LED is grounded. At this time the LED is on, while the output voltage terminal of V1>V2 and V1<V2, namely the electrical potential of G terminal is zero. Both V1>V2 and V1<V2 terminals are serial connected with unilateral diode D50 to G terminal. When V1≠V2, G terminal can receive a positive output, and is further coupled with a grounding resistor R53, functioning to keep G terminal at zero potential. The preferred embodiment is characterised by an additional set of V1=V2 equilibrium indicator and an additional DCIC, and the power supply voltage Vn to the DCIC

is contingent upon the choice of IC variety without limitation. In this preferred embodiment, the DCIC may be replaced with up and down limit comparators.

As shown in Fig. 12, the balance resistor VR capable of equilibrium tuning applied in Fig. 8 schematic is allocated from the limit current resistor R2 to connect to the circuit of the measure resistor R1, characterised by the two ends of the variable resistor VR are connected to the measure resistor R1, and the mid point to B point, and concurrently the mid point of the two limit current resistors R2 is also connected to B point. The function is suited for CCFL clusters of small consumption. In this preferred embodiment, the DAIC may be replaced with up and down limit comparators.

As shown in Fig. 13, the balance resistor VR capable of equilibrium tuning applied in Fig. 9 schematic is allocated from the limit current resistor R1 to connect to the circuit of the measure resistor R2, characterised by the two ends of the variable resistor VR are connected to the measure resistor R1, and the mid point to B point, and concurrently the mid point of the two limit current resistors R2 is also connected to B point. The function is suited for CCFL clusters of small consumption. In this preferred embodiment, the DCIC may be replaced with up and down limit comparators.

As shown in Fig. 14 the tenth exemplary schematic of the preferred embodiment, the serial connection of the secondary of the photocouplers Ph1, Ph2, Ph3...Phn is altered to independent photocoupler circuits. The schematic of Fig. 14 shows that each photocoupler Ph1, Ph2, Ph3...Phn has a negative resistor R14 and unilateral output diode D33. One end of the negative resistor R14 is connected directly to power source B+, the other end to the collect-emitter terminal of the photocoupler secondary and the P-type terminal of unilateral diode D33. The emitter terminal of the photocoupler secondary is connected to the negative terminal of the DC power, while the N-type terminal of the unilateral diode D33 is conjoined with all the N-type terminals of unilateral diode D33 of all photocouplers Ph1, Ph2, Ph3...Phn, and further connected to the noninverter terminal of the up limit comparator OP1 and the inverter terminal of the down up limit comparator OP2. The functioning principle is that when CCFLs L1, L2, L3...Ln on the AB terminal are functioning normally, the N-type terminal of the unilateral diode D33 has no output voltage; the noninverter terminal of the up limit comparator OP1 and the N-type terminal of the unilateral diode D33 are

joined together as when the voltage at the noninverter terminal of the up limit comparator OP1 is zero, the output terminal G is zero voltage. If any CCFL of CCFL Cluster L1, L2, L3...Ln open-circuits, the noninverter terminal of the up limit comparator OP1 will have a positive voltage, enabling the output terminal G to have a positive voltage that subject voltage to thyristor of SCR220 of the electronic ballast 200, resulting in eliminating HF voltage at the A and B terminals to achieve protection of CCFL quality.

As shown in Fig. 15 the eleventh exemplary schematic of the preferred embodiment, if the lamp current of CCFL Cluster L1, L2, L3...Ln is smaller than the LED current of the photocouplers Ph1, Ph2, Ph3...Phn, the LED of the photocouplers may be directly connected to the circuit, namely changing Fig. 14 schematic to the one presented in Fig. 15. The functioning principle of Fig. 15 is the same as Fig. 14, but simplified, provided the premises being that the current borne by photocoupler LED shall be greater than the CCFL current to deter burning photocoupler LED.

As shown in Fig. 16 the twelfth exemplary schematic of the preferred embodiment, the schematic is a reconfiguration of Fig. 6 schematic's measure resistor R1 and bridge rectifier BR. The functioning principle lies with the two AC terminals of the bridge rectifier BR are connected to L1 and L2 measure resistor R1. When the lamp current of the two CCFL clusters L1 and L2 is the same, the positive and negative terminals of the bridge rectifier BR will be zero concurrently. If the current of the two CCFL clusters L1 and L2 is different, the potentials of the positive and negative terminals of the bridge rectifier BR will be different, ensuing a voltage. This voltage travels from the positive terminal through the limit current resistor R2 to reach the LED terminal of the photocoupler Ph. At this time, the secondary collect-emitter terminal of the photocoupler Ph is conducted, DC power BHF passing through the limit current resistor R30, then the collect-emitter of the photocoupler Ph to reach the positive terminal of the up limit comparator OP1 and the negative end of the down limit comparator OP2. At this time the output terminal G of the comparators has a positive current output to eliminate the HF voltage at AB terminal in achieving the goal of protecting CCFL cluster function and quality. The circuit is characterised by L1 and L2, L3, and L4, L5 and L6, ...Ln-1 and Ln, every pair of CCFLs share a bridge rectifier BR, and all the positive terminals of the bridge

rectifiers BR are connected together, and all the negative terminals of the bridge rectifiers BR are also connected together.

In summarising the foregoing, the preferred embodiment pertains to a type of device for measuring and protecting CCFL, mainly utilising a type of electronic ballast to serve as HF power source for the backlighting of multiple cold cathode fluorescent lamps by means of serial connect one end of each cold cathode fluorescent lamp of parallel connected CCFL Cluster with a measure element; said element provides power source for the photocoupler LED. Concurrently, the photocouplers' collect-emitter terminals are joined in serial connection, and then employ comparators to determine any short circuit, over current, or under current occurred within the CCFL Cluster, thus protecting the cold cathode fluorescent lamps to achieve large LCD monitors' quality requirement and performance protection.

Scope of claim

1. A type of measure device for cold cathode fluorescent lamps, which comprises:

High frequency power source circuit: utilising AC power source;

Time delay circuit: when the electronic ballast is working stably, an that the cold cathode fluorescent lamps are in full brightness and stable, there is a pause before determining the electronic ballast's "on", "off" status; the functioning time thus deferred is contingent upon the number, characteristic and quality of the CCFL Cluster;

DC power source circuit: the output terminal's DC voltage supplies the CCFL Cluster, the protect circuit, and the time delay circuit, or internal, external power supply from other independent system;

CCFL set: comprises HF HV capacitor, cold cathode fluorescent lamps, measure resistor, limit current resistor and photocoupler primary; multiple CCFL sets are joined together by parallel connection to form a CCFL Cluster. To accommodate backlighting required by large LCD monitors, multiple clusters may be conjoined, characterised by serial connection of HV capacitors and cold cathode fluorescent lamps and measure resistors; the two terminals are the connected to HF HV